DATA STORAGE DEVICE, METHOD OF OPERATING THE SAME, AND DATA PROCESSING SYSTEM INCLUDING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority under 35 U.S.C. §119(a) from Korean Patent Application No. 10-2015-0106733, filed on Jul. 28, 2015 in the Korean Intellectual Property Office, the disclosure of which is hereby incorporated by reference in its entirety.

BACKGROUND

[0002] Apparatuses and methods consistent with exemplary embodiments relate to a data storage device, and more particularly, to a data storage device for realizing parallel executions, a method of operating the same, and a data processing system including the same.

[0003] Memory devices may be categorized as volatile memory devices and non-volatile memory devices. Volatile memory devices maintain data while the device is powered, whereas non-volatile memory devices maintain data even after having been power cycled.

[0004] A flash memory device is an example of electrically erasable programmable read-only memory (EEPROM) in which a plurality of memory cells are erased or programmed in one program operation.

[0005] A flash translation layer (FTL) is software for efficiently managing a flash memory device. The FTL is included in a memory controller and translates a logical address into a physical address of the flash memory device. The FTL has a mapping table for the translation. The mapping table includes information about mapping between a logical address and a physical address.

[0006] When a drive includes flash memory devices, the number of flash memory devices needs to be increased in order to increase the capacity of the drive. As the number of flash memory devices included in the drive increases, the capacity or size of a mapping table also needs to be increased. Due to capacity and processing speed of memory storing the mapping table, the number of flash memory devices may be limited. In other words, when a memory resource is not sufficient for the FTL to load all mapping tables, mapping tables are loaded as needed during the operation of a flash memory device. As a result, the input/output performance of the drive may deteriorate.

SUMMARY

[0007] According to an aspect of an exemplary embodiment, there is provided a data storage device including: a non-volatile memory device; and a controller configured to receive a command from a host and to control an operation of the non-volatile memory device based on the command, the controller including a processor configured to receive and process the command and an address extractor configured to extract address information from the command and to output the address information to the processor before the processor processes the command.

[0008] The processor may include: a first core configured to generate a sub-command based on the command; and a plurality of second cores configured to receive the sub-command output from the first core.

[0009] The sub-command may correspond to commands for controlling peripheral devices comprised in the data storage device to perform one among a read operation and a write operation of the non-volatile memory device.

[0010] The sub-command may correspond to one among a read operation, a write operation, and a trimming operation on peripheral devices comprised in the data storage device.

[0011] The address information may include logical address information corresponding to peripheral devices comprised in the data storage device.

[0012] The logical address information may include a namespace, a volume, a logical block address, and a length.

[0013] The first core may be configured to determine the command at a first time point and the address extractor may be configured to output the address information to the plurality of second cores at the first time point.

[0014] The plurality of second cores may be configured to perform an operation of preparing to control peripheral devices comprised in the data storage device at the first time point based on the address information.

[0015] The plurality of second cores are configured to determine, at the first time point, whether internal management data corresponding to the address information has been loaded to the controller; and load, in response to the determining indicating the internal management data has not been loaded, the internal management data corresponding to the address information from the non-volatile memory device at a second time point after the first time point.

[0016] The sub-command may comprise a command corresponding to an operation of loading the internal management data corresponding to the address information and a command corresponding to an operation of programming the non-volatile memory device based on the internal management data.

[0017] The internal management data may include map information corresponding to the address information among information corresponding to a logical address and a physical address which are comprised in a mapping table of the non-volatile memory device.

[0018] Each of the plurality of second cores may be configured to determine whether to process the received sub-command based on the address information.

[0019] The address information may indicate a selected second core of the plurality of second cores, and only the selected second core processes the received sub-command.

[0020] According to an aspect of another exemplary embodiment, there is provided a method of operating a data storage device including a first core, a plurality of second cores and a non-volatile memory device, the method including: receiving a command from a host; extracting address information from the command; determining whether a target designation mode has been set based on the address information extracted from the command; transmitting a request including the address information to the plurality of second cores; and processing, by the first core, the command to generate a sub-command.

[0021] The method may further include determining whether the plurality of second cores support a queue format after the determining whether the target designation mode has been set; forming a queue including the request, in response to determining the plurality of second cores support the queue format; and transmitting the request in the queue to the plurality of second cores.